MOTOROLA

MC12014

COUNTER CONTROL LOGIC

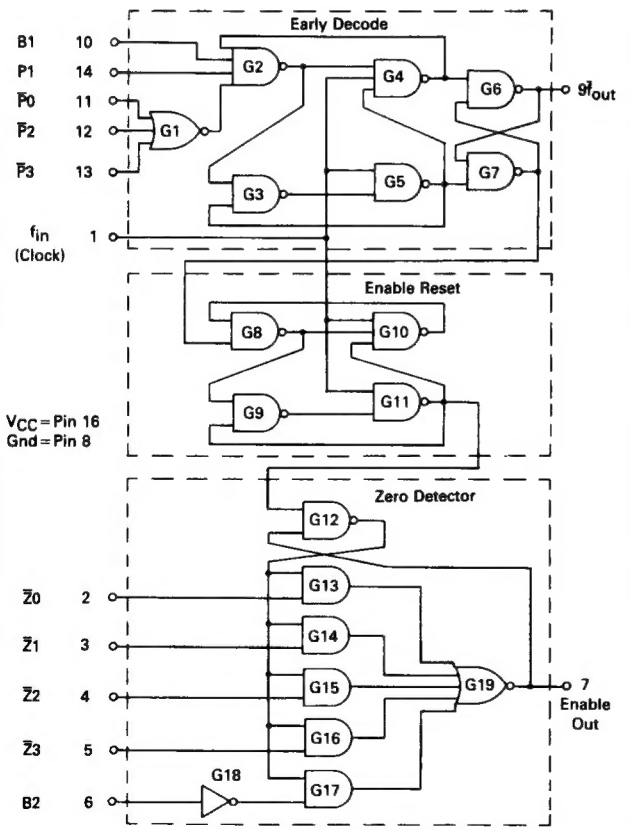
The MC12014 monolithic counter control logic unit is designed for use with the MC12013 Two-Modulus Prescaler and the MC4016 Programmable Counter to accomplish direct high-frequency programming. The MC12014 consists of a zero detector which controls the modulus of the MC12013, and an early decode function which controls the MC4016. The early decode feature also increases the useful frequency range of the MC4016 from 8.0 MHz to 25 MHz.

COUNTER CONTROL LOGIC

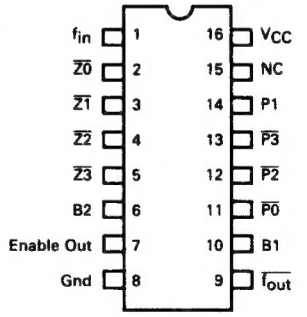
P SUFFIX
PLASTIC PACKAGE
CASE 648

L SUFFIX
CERAMIC PACKAGE
CASE 620

LOGIC DIAGRAM



PIN ASSIGNMENT



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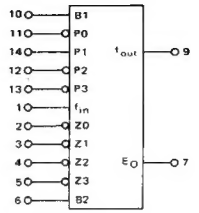
ELECTRICAL CHARACTERISTICS

Test procedures are shown for the f_{in}, $\overline{Z}0$, B1 and P1 inputs. All other inputs are tested in the same manner as the $\overline{Z}0$ input.



Characteristic	Symbol	Pin Under Test	Test Limits 0 to +75°C Min	Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW. I_{OL} (mA)	I_{OH} (mA)	I_{IC} (mA)	V_{IL} (Volts)	V_{IH} (Volts)	V_{IHH} (Volts)	V_{RH} (Volts)	V_{CC} (Volts)	V_{CCL} (Volts)	V_{CCH} (Volts)	Gnd
						TEST CURRENT/VOLTAGE VALUES (All Temperatures)										
						mA			Volts							
						I_{OL}	I_{OH}	I_{IC}	V_{IL}	V_{IH}	V_{IHH}	V_{RH}	V_{CC}	V_{CCL}	V_{CCH}	
						16	-1.6	-10	0.5	2.4	5.5	4.5	5.0	4.75	5.25	
Input																
Forward Current	I_{IL}	1	–	-6.4	mAdc	–			1	–	–	–	–	–	16	8,10
		2	–	-1.6	↓	–	–	–	2	–	–	–	–	–	↓	8
		10	–	↓	↓	–	–	–	10	–	–	–	–	–	↓	1,8,11,12,13
		14	–	↓	↓	–	–	–	14	–	–	–	–	–	↓	1,8,11,12,13
Leakage Current	I_{IH}	1	–	160	μAdc	–	–	–	–	1	–	–	–	–	16	8,10
		2	–	40	↓	–	–	–	–	2	–	–	–	–	↓	8
		10	–	↓	↓	–	–	–	–	10	–	–	–	–	↓	1,8,11,12,13
		14	–	↓	↓	–	–	–	–	14	–	–	–	–	↓	1,8,11,12,13
	I_{IHH}	1	–	1.0	mAdc	–	–	–	–	–	1	–	–	–	16	8
		2	–	↓	↓	–	–	–	–	–	2	–	–	–	↓	8
		10	–	↓	↓	–	–	–	–	–	10	–	–	–	↓	1,8,11,12,13
		14	–	↓	↓	–	–	–	–	–	14	–	–	–	↓	1,8,11,12,13
Clamp Voltage	V_{IC}	1	–	-1.2	Vdc	–	–	1	–	–	–	–	–	16	–	8
		2	–	↓	↓	–	–	2	–	–	–	–	–	↓	–	↓
		10	–	↓	↓	–	–	10	–	–	–	–	–	↓	–	↓
		14	–	↓	↓	–	–	14	–	–	–	–	–	↓	–	↓
Output																
Output Voltage	V_{OL}*	7	–	0.5	Vdc	7	–	–	11,12,13	–	–	2,3,4,5,10,11	–	16	–	8
		9	–	0.5	Vdc	9	–	–	11,12,13	–	–	10,14	–	16	–	8
	V_{OH}	7	2.4	–	Vdc	–	7	–	2,3,4,5	–	–	6	–	16	–	8
		9**	2.4	–	Vdc	–	9	–	–	–	–	11,12,13	–	16	–	8
Short-Circuit Current	I_{OS}	7	-20	-65	Vdc	–	–	–	2,3,4,5	–	–	6	16	–	–	7,8
		9**	-20	-65	Vdc	–	–	–	–	–	–	11,12,13	16	–	–	8,9
Power Requirements																
Power Supply Drain	I_{CC}	16	–	35	mAdc	–	–	–	–	–	–	–	16	–	–	1,8

*Output level to be measured after waveform 1 is applied to f_{in}, pin 1.
**Output level to be measured after waveform 2 is applied to f_{in}, pin 1.

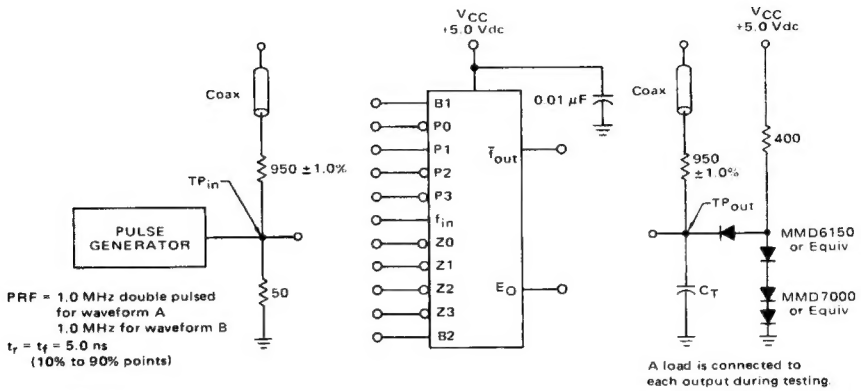
Waveform 1: 

Waveform 2: 

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc, waveform letters refer to waveforms on next page.)

Characteristic	Symbol	Pin Under Test		Test Limits (ns)							Pulse Gen. 1		Pulse Gen. 2		Pulse Out		Voltage Applied to Pins Listed Below	
				0°C		+25°C			+75°C									
		In	Out	Min	Max	Min	Typ	Max	Min	Max	Wave-form	Pin	Wave-form	Pin	Wave-form	Pin	V_{IL} = 0.5 V	V_{IH} = 2.4 V
Propagation Delay	t_{PLH1}	1	9	7.0	15	7.0	10	15	7.0	17	A	1	J	10	K	9	11,12,13	14
	t_{PHL1}	1	9	7.0	16	7.0	11	16	7.0	18	A	1	J	10	K	9	11,12,13	14
	t_{PLH2}	2	7	5.0	12	5.0	8.5	12	5.0	14	A	1	H	2	L	7	3,4,5,11,12,13	6,10,14
		3	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	3	↓	↓	2,4,5,11,12,13	↓
		4												4			2,3,5,11,12,13	
		5												5			2,3,4,11,12,13	
	t_{PHL2}	1	7	7.0	16	7.0	11	16	7.0	18	A	1	H	2	L	7	3,4,5,11,12,13	6,10,14
	t_{PLH3}	6	7	7.0	16	7.0	11	16	7.0	18	A	1	J	6	L	7	2,3,4,5,11,12,13	10,14
Setup Time	t_{setup}"1"	10	–	–	–	–	1.0	2.0	–	–	A	1	B	10	G	9	11,12,13	14
		11	–	–	–	–	7.0	12	–	–				11	F		12,13	10,14
		12	–	–	–	–	↓	↓	–	–				12	↓		11,13	↓
		13	–	–	–	–			–	–				13			11,12	
		14	–	–	–	–	1.0	2.0	–	–				14	G		11,12,13	10
	t_{setup}"0"	10	–	–	–	–	4.5	8.0	–	–	A	1	C	10	F	9	11,12,13	14
		11	–	–	–	–	5.0	9.0	–	–				11	G		12,13	10,14
		12	–	–	–	–	↓	↓	–	–				12	↓		11,13	↓
		13	–	–	–	–			–	–				13			11,12	
		14	–	–	–	–	4.5	8.0	–	–				14	F		11,12,13	10
Hold Time	t_{hold}"1"	10	–	–	–	–	4.0	8.0	–	–	A	1	D	10	G	9	11,12,13	14
		11	–	–	–	–	5.0	10	–	–				11	F		12,13	10,14
		12	–	–	–	–	↓	↓	–	–				12	↓		11,13	↓
		13	–	–	–	–			–	–				13			11,12	
		14	–	–	–	–	4.0	8.0	–	–				14	G		11,12,13	10
	t_{hold}"0"	10	–	–	–	–	1.0	2.0	–	–	A	1	E	10	F	9	11,12,13	14
		11	–	–	–	–	7.5	14	–	–				11	G		12,13	10,14
		12	–	–	–	–	↓	↓	–	–				12	↓		11,13	↓
		13	–	–	–	–			–	–				13			11,12	
		14	–	–	–	–	1.0	2.0	–	–				14	F		11,12,13	10

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

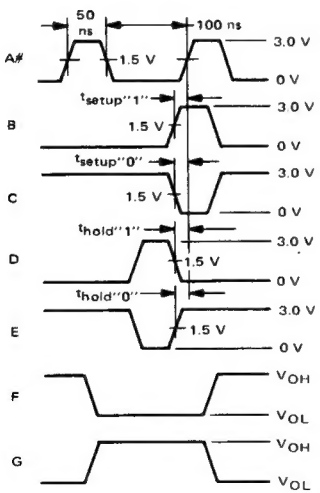


Two pulse generators are required and must be slaved together to provide the waveforms shown.

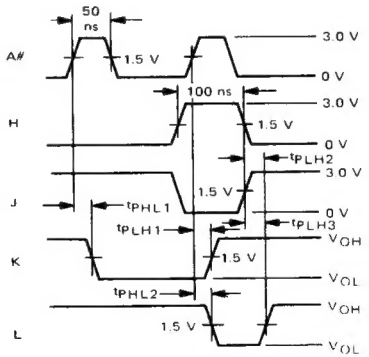
C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

SETUP AND HOLD TIMES



PROPAGATION DELAY TIMES



#Pulse A (f_{in}) used with all tests.

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APPLICATIONS INFORMATION

The MC12014 Counter Control Logic incorporates two features for enhancing operation of the MC4016/4018 Programmable Counters.[1] Maximum operating frequency of the counters is limited by the time required for re-programming at the end of each count-down cycle. Operation can be extended to approximately 25 MHz by using the "early decode" feature included in the MC12014. The appropriate connections are shown in Figure 2. Only three counter stages are shown; however, up to eight stages can be satisfactorily cascaded. Note the following differences between this and the non-extended method: the counter gate inputs are not connected to the input clock; all parallel enables are connected to the $\overline{Q}$ output (f_{out}) of a type D flip-flop formed by gates G2 through G7 in the MC12014 package; the bus terminal of the least significant stage is grounded; all other bus terminals and one internal resistor, R, are connected together and serve as a data input, B1, to the flip-flop. Four additional data inputs, $\overline{P}0$ through $\overline{P}3$, serve to decode the "two" state of the least significant counter stage. Circuit operation is illustrated in waveforms of Figure 2, where the timing for the end of a count-down cycle is shown in expanded form. The counter parallel inputs are assumed to have N = 245 programmed. Timing is not shown for the third stage since it has already been counted down to the all zero state. As the next-to-least significant stage reaches zero, the common bus line goes high. Count down of the least significant stage continues until the "two" state is reached, causing the remaining data inputs to the flip-flop to go high. The next-to-last clock pulse of the cycle then triggers the flip-flop $\overline{Q}$ output low. This takes the parallel enables of all three counter stages low, resetting the programmed data to the outputs. The next input pulse clocks $\overline{Q}$ back to the high state since the data inputs to the flip-flop are no longer all high. The resulting negative output pulse at f_{out} is one input clock period in duration. Note that division by N equal to 001 or 002 is not available using this method.

The frequency synthesizer shown in Figure 8 requires that the programmable counters be quickly stopped after reaching their terminal (zero) count. This can be simply accomplished by taking the master reset of all stages low at the appropriate time. The bus output of the counters could be used for this function since a transition there signals the end of a count-down sequence. However, due to the relatively long delay between the last positive clock transition and the bus transition a faster method is required in this application.

The "zero detection" feature of the MC12014 provides a convenient means of implementing a faster method. Gates G12 through G19 form a latch whose output goes high if B2 is high and low logic levels are applied to the Z0 thru Z3 inputs. When once set to a one by appropriate input conditions, the output of G19 remains high until it is reset by the circuit comprised of gates G8 through G11. Note that since the required information is stored, the counter can be allowed to continue cycling.

The G8-G11 circuit monitors the G7 output of the "early decode" type D flip-flop. When the counter stage connected to the $\overline{P}0$ thru $\overline{P}3$ inputs has counted down to its two state the output of G7 goes high; this enables the G8-G11 circuitry and the next positive clock transition causes the output of G11 to go high, resetting the output of G19 to zero.

FIGURE 1 — TYPICAL FREQUENCY SYNTHESIZER APPLICATION

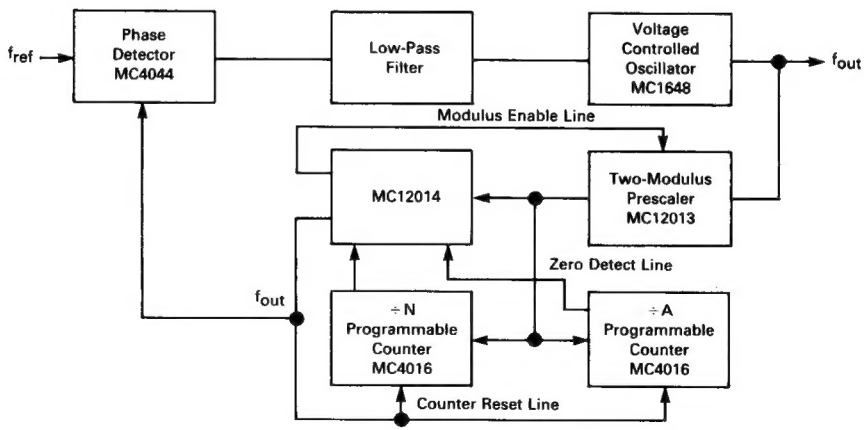
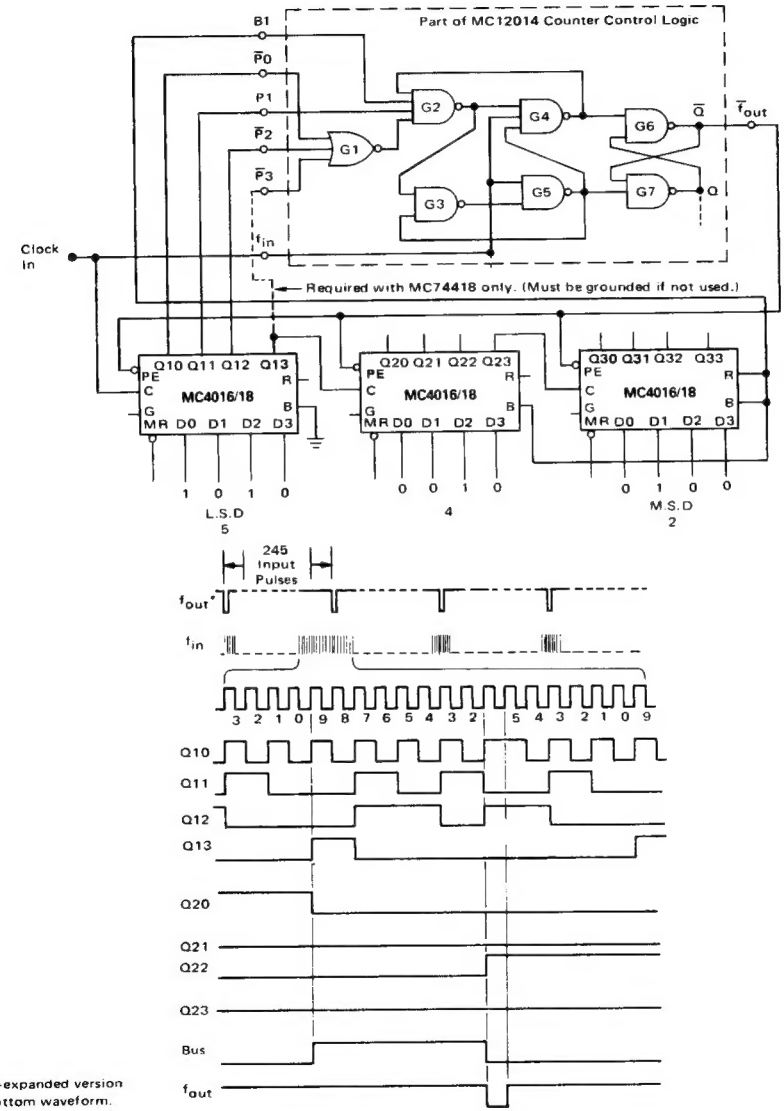


FIGURE 2 — INCREASING THE OPERATING RANGE OF MC74416/74418 PROGRAMMABLE COUNTERS USING MC12014



1 See the MC54416/54418 data sheet for additional information.

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Operation of the Counter Control Logic can be further clarified by considering a typical system application for programmable counters illustrated in the frequency synthesizer shown in Figure 3. There the counter provides a means of digitally selecting some integral multiple of a stable reference frequency. The circuit phase locks the output, f_{VCO}, of a voltage controlled oscillator to a reference frequency, f_{ref}.[2] Circuit operation is such that $f_{VCO} = Nf_{ref}$, where N is the divider ratio of the feedback counter, permitting frequency selection by means of thumbwheel switches.

In many synthesizer applications the VCO is operated at VHF frequencies too high for direct division by TTL counters. In these cases the VCO output is usually prescaled by using a suitable fixed divide-by-M ECL circuit as shown in Figure 4. For this configuration, $f_{VCO} = NMf_{ref}$, where N is variable (programmable) and M is fixed. Design of the optimum loop filter requires that the input reference frequency be as high as possible where the upper limit is established by the required channel spacing. Since $f_{VCO} = Nf_{ref}$ in the non-prescaled case, if N is changed by one, the VCO output changes by f_{ref}, or the synthesizer channel spacing is just equal to f_{ref}. When the prescaler is used as in Figure 4, $f_{VCO} = NMf_{ref}$, and a change of one in N results in the VCO changing by Mf_{ref}, i.e., if f_{ref} is set equal to the minimum permissible channel spacing as is desirable, then only every M channels in a given band can be selected. One solution is to set f_{ref} = channel spacing/M but this leads to more stringent loop filter requirements.

FIGURE 3 — TTL PHASE-LOCKED LOOP

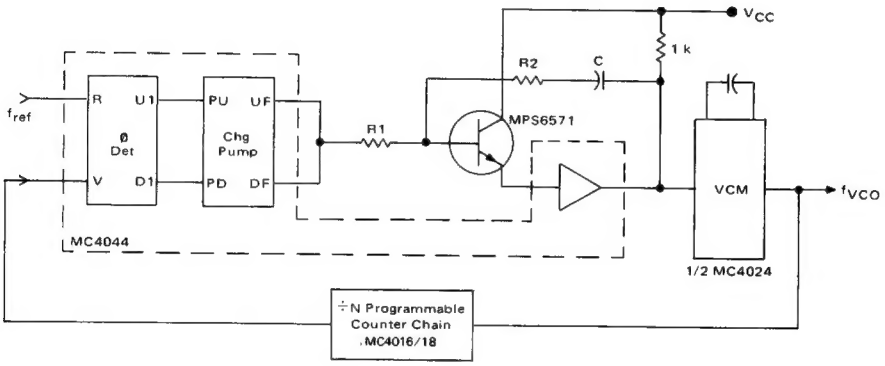
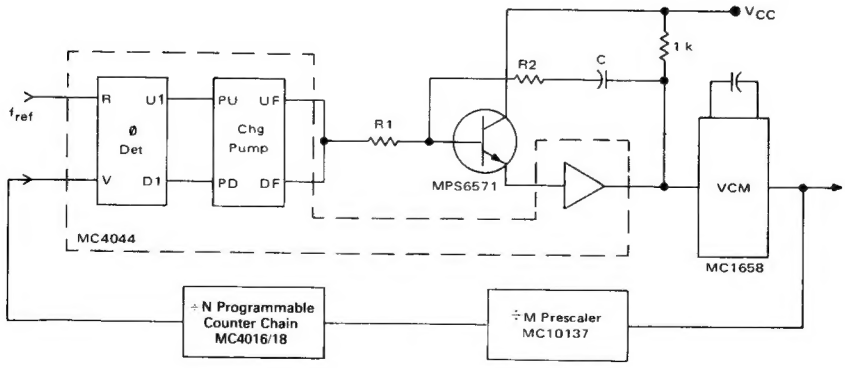


FIGURE 4 — TTL-MECL PHASE-LOCKED LOOP



2 See Motorola Application Notes AN-535, AN-532, and the MC4344/4044 Data Sheet for detailed explanation of over-all circuit operation.

An alternate approach that avoids this problem is provided by the counter configuration shown in Figure 5. It too uses a prescaler ahead of a programmable counter, however the modulus of the prescaler is now controlled by a third counter, causing it to alternate between M and M + 1. Operation is best explained by assuming that all three counters have been set for the beginning of a cycle: the prescaler for division by (M + 1), the modulus control counter for division by N_{mc}, and the programmable counter for division by N_{pc}. The prescaler will divide by (M + 1) until the modulus control counter has counted down to zero; at this time, the all zero state is detected and causes the prescaler to divide by M until the programmable counter has also counted down to zero. When this occurs, a cycle is complete and each counter is reset to its original modulus in readiness for the next cycle.

To determine the relationship between f_{out} and f_{in}, let T_1 be the time required for the modulus control counter to reach its terminal count and let T_2 be the remainder of one cycle. That is, T_2 is the time between terminal count in the modulus control counter and terminal count in the programmable counter. When the modulus control counter reaches zero, N_{mc} pulses will have entered it at a rate given by $f_{in}/(M + 1)$ pulses/second or T_2 is:

$$T_1 = \frac{(M + 1)}{f_{in}} \cdot N_{mc} \qquad (1)$$

At this time, N_{mc} pulses have also entered the programmable counter and it will reach its terminal counter after $(N_{pc} - N_{mc})$ more pulses have entered. The rate of entry is now f_{in}/M pulses/second since the prescaler is now dividing by M. From this T_2 is given by:

$$T_2 = \frac{M}{f_{in}} \cdot (N_{pc} - N_{mc}) \qquad (2)$$

Since $f = \frac{1}{T}$:

$$f_{out} = \frac{1}{T_{total}} = \frac{1}{T_1 + T_2} = \frac{1}{\frac{(M+1)N_{mc}}{f_{in}} + \frac{M(N_{pc} - N_{mc})}{f_{in}}} \qquad (3)$$

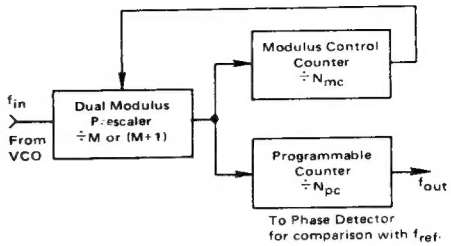
$$f_{out} = \frac{f_{in}}{(M+1)N_{mc} + M(N_{pc} - N_{mc})}$$

$$= \frac{f_{in}}{MN_{mc} + N_{mc} + MN_{pc} - MN_{mc}}$$

$$= \frac{f_{in}}{MN_{pc} + N_{mc}}$$

In terms of the synthesizer application, $f_{VCO} = (MN_{pc} + N_{mc})\, f_{ref}$ and channels can be selected every f_{ref} by letting N_{pc} and N_{mc} take on suitable integer values, including zero.

FIGURE 5 — FEEDBACK COUNTERS WITH DUAL MODULUS PRESCALER



A simplified example of this technique is shown in Figure 6. The MC12013 Dual Modulus Prescaler divides by either 10 or 11 when connected as shown in Figure 6. If the E3 and E4 Enable inputs are high at the start of a prescaler cycle, division by 10 results; if the Enable inputs are low at the beginning of the cycle, division by 11 results. The zero detection circuitry of the MC12014 Counter Control Logic is connected to monitor the outputs of the modulus control counter; this provides a suitable enable signal at E0 as the modulus control counter reaches its terminal (zero) count. The remainder of the MC12014 is connected to extend the operating frequency of the programmable counter chain. Appropriate waveforms for division by 43 are shown in Figure 7a.

The beginning of the timing diagram indicates circuit status just prior to the end of a countdown cycle, i.e., the modulus control counter has been counted down to one and the programmable counter is in the two state. The next positive transition from the prescaler (f1 in the timing diagram) then initiates the following sequence of events. Since the two state of the programmable counter enables the early decode circuitry in the MC12014, the positive f1 transition causes f_{out} to go low. Since f_{out} is connected to the Parallel Enables of all the MC4016 counters this low signal will re-program the counters in readiness for another cycle. However, due to the propagation time through the decode circuitry, the programmable and modulus control counters are briefly decremented to one and zero, respectively, before reprogramming occurs. The momentary zero state of the modulus control counter is detected, setting E_O of the MC12014 high, enabling the MC12013 for division by ten during its next cycle. After eleven more f_{in} pulses (E_O went high after the beginning of the prescaler cycle and so doesn't change the modulus until the next prescaler cycle), f1 again goes high, causing f_{out} to return to the one state. This releases the Parallel Enables and simultaneously resets E_O to zero. However, since E_O was high when the current prescaler cycle began, the next positive f1 transition occurs only ten f_{in} pulses later. Subsequent f1 transitions now decrement the MC4016 counters down through another cycle with the prescaler dividing by eleven. From the waveforms, 11 + 10 + 11 + 11 = 43 input pulses occur for each output pulse.

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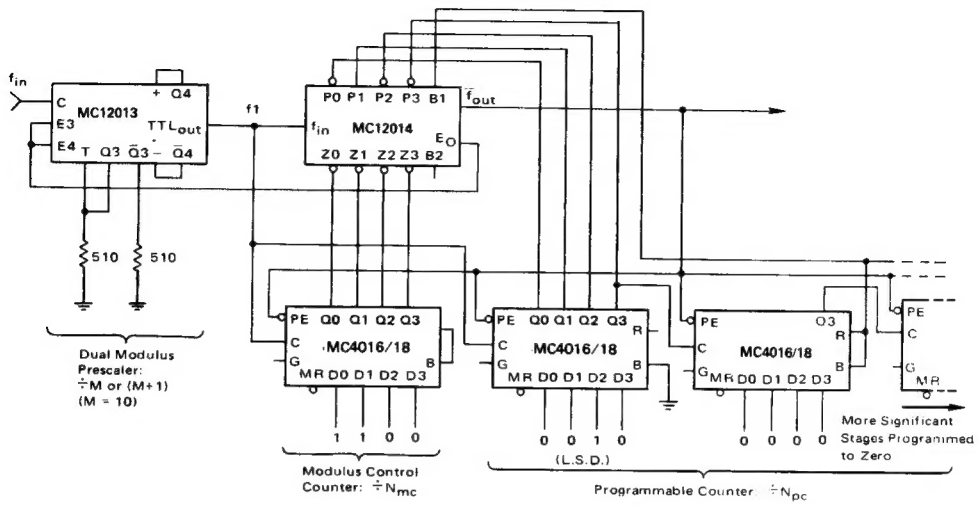
FIGURE 6 — FREQUENCY DIVISION: $f_O = f_{in}/(MN_{pc} + N_{mc})$



Division by 42 is shown in Figure 7b. Operation is similar except that the modulus control counter reaches its terminal count one f1 cycle earlier than before. Since E_O is reset by the trailing edge of the f_{out} pulse, E_O now remains high for two prescaler cycles leading to 10 + 10 + 11 + 11 = 42 input pulses for each output pulse.

Other combinations lead to similar results, however note that N_{pc} must be greater than or equal to N_{mc} for operation as described. If N_{mc} is greater than N_{pc} erroneous results are obtained, however this is not a serious restriction since N_{pc} is greater than N_{mc} in most practical applications.

The synthesizer shown in Figure 8 generates frequencies in the range from 144 to 178 MHz with 30 kHz channel spacing. It uses the dual modulus prescaler approach discussed earlier. General synthesizer design considerations are detailed in the publications listed in footnote 2, hence only the feedback counter is discussed here. Requirements for the feedback divider are determined from:

$$\text{Minimum Divider Ratio} = N_{Tmin} = \frac{144.00\ \text{MHz}}{30\ \text{kHz}} = 4800$$

$$\text{Maximum Divider Ratio} = N_{Tmax} = \frac{177.99\ \text{MHz}}{30\ \text{kHz}} = 5933$$

If the prescaler divides by at least ten, the maximum input frequency to the TTL counters will be 17.799 MHz, allowing use of MC4016 Programmable Counters with the MC12014 frequency extension feature.

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FIGURE 7a — DIVISION BY 43

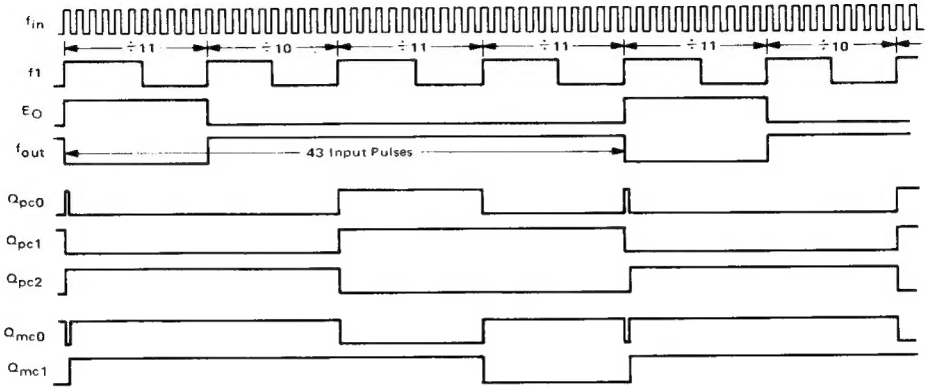
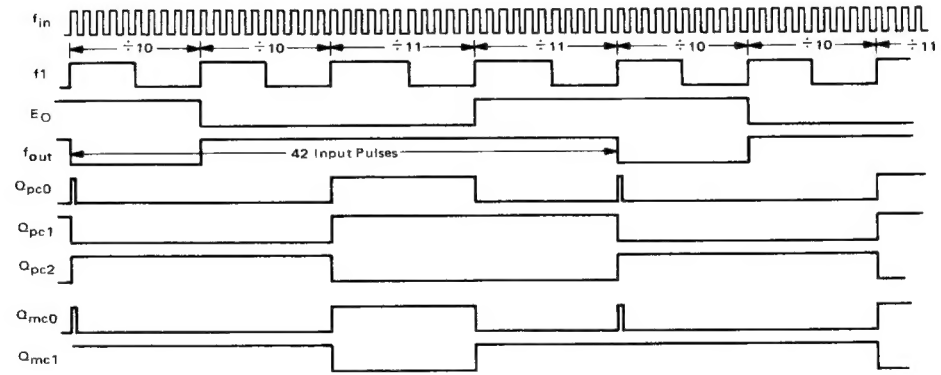


FIGURE 7b — DIVISION BY 42



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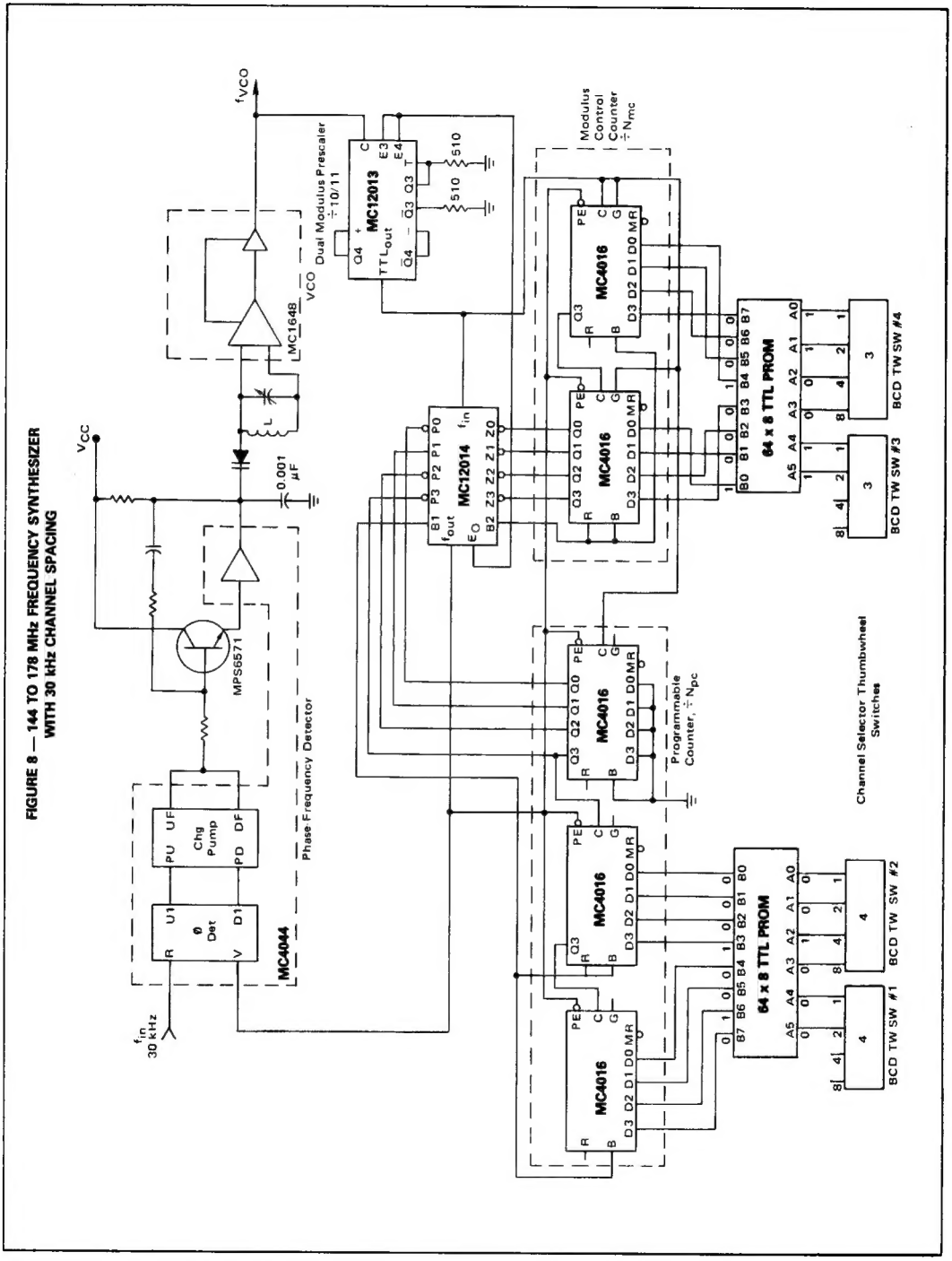

FIGURE 8 — 144 TO 178 MHz FREQUENCY SYNTHESIZER WITH 30 kHz CHANNEL SPACING

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FIGURE 9 — N_{pc} PROM PROGRAMMING

	SW #1	SW #2	SW #1 A5	SW #1 A4	SW #2 A3	SW #2 A2	SW #2 A1	SW #2 A0	PROM WORD	PROM OUTPUT M.S.B.			PROM OUTPUT L.S.B.				N_{pc}	
(144 MHz)	44		0	0	0	0	0	0	4	0	0	0	1	0	0	0	48	480
	45		0	0	0	0	0	1	5	0	0	0	1	0	0	0	48	
	46		0	0	0	0	1	0	6	0	0	0	1	0	0	0	48	
	47		0	0	0	0	1	1	7	0	0	0	1	0	0	1	49	
	48		0	0	0	1	0	0	8	0	0	0	1	0	0	1	49	
	49		0	0	0	1	0	1	9	0	0	0	1	0	0	1	49	
	50		0	0	1	0	0	0	16	0	0	0	1	0	0	0	50	
	51		0	0	1	0	0	0	17	0	0	0	1	0	0	0	50	
	52		0	0	1	0	0	1	18	0	0	0	1	0	0	0	50	
	53		0	0	1	0	0	1	19	0	0	0	1	0	0	0	51	
	54		0	0	1	0	1	0	20	0	0	0	1	0	0	1	51	
	55		0	0	1	0	1	1	21	0	0	0	1	0	0	1	51	
	56		0	0	1	0	1	1	0	22	0	0	0	1	0	0	1	0	52	
	57		0	0	1	0	1	1	1	23	0	0	0	1	0	0	1	0	52	
	58		0	0	1	1	0	0	0	24	0	0	0	1	0	0	1	0	52	
	59		0	0	1	1	0	0	1	25	0	0	0	1	0	0	1	1	53	
	60		0	0	1	1	0	0	0	32	0	0	0	1	0	0	1	1	53	
	61		0	0	1	1	0	0	0	1	33	0	0	0	1	0	0	1	1	53
	62		0	0	1	1	0	0	1	0	34	0	0	0	1	0	1	0	0	54
	63		0	0	1	1	0	0	1	1	35	0	0	0	1	0	1	0	0	54
	64		0	0	1	1	0	1	0	0	36	0	0	0	1	0	1	0	0	54
	65		0	0	1	1	0	1	0	1	37	0	0	0	1	0	1	0	1	55
	66		0	0	1	1	0	1	1	0	38	0	0	0	1	0	1	0	1	55
	67		0	0	1	1	0	1	1	1	39	0	0	0	1	0	1	0	1	55
	68		0	0	1	1	1	0	0	0	40	0	0	0	1	0	1	1	0	56
	69		0	0	1	1	1	0	0	1	41	0	0	0	1	0	1	1	0	56
	70		0	0	1	1	1	0	0	0	48	0	0	0	1	0	1	1	0	56
	71		0	0	1	1	1	0	0	1	49	0	0	0	1	0	1	1	1	57
	72		0	0	1	1	1	0	0	1	0	50	0	0	0	1	0	1	1	1	57
	73		0	0	1	1	1	0	0	1	1	51	0	0	0	1	0	1	1	1	57
	74		0	0	1	1	1	0	1	0	0	52	0	0	0	1	1	0	0	0	58
	75		0	0	1	1	1	0	1	0	1	53	0	0	0	1	1	0	0	0	58
	76		0	0	1	1	1	0	1	1	0	54	0	0	0	1	1	0	0	0	58
(177 MHz)	77		0	0	1	1	1	0	1	1	1	55	0	0	0	1	1	0	0	1	59	590

WORD	BIT 7	6	5	4	3	2	1	0
0	–	–	–	–	–	–	–	–
1	–	–	–	–	–	–	–	–
2	–	–	–	–	–	–	–	–
3	–	–	–	–	–	–	–	–
4	0	1	0	0	1	0	0	0
5	0	1	0	0	1	0	0	0
6	0	1	0	0	1	0	0	0
7	0	1	0	0	1	0	0	1
8	0	1	0	0	1	0	0	1
9	0	1	0	0	1	0	0	1
10	–	–	–	–	–	–	–	–
11	–	–	–	–	–	–	–	–
12	–	–	–	–	–	–	–	–
13	–	–	–	–	–	–	–	–
14	–	–	–	–	–	–	–	–
15	–	–	–	–	–	–	–	–
16	0	1	0	1	0	0	0	0
17	0	1	0	1	0	0	0	0
18	0	1	0	1	0	0	0	0
19	0	1	0	1	0	0	0	1
20	0	1	0	1	0	0	0	1
21	0	1	0	1	0	0	0	1
22	0	1	0	1	0	0	1	0
23	0	1	0	1	0	0	1	0
24	0	1	0	1	0	0	1	0
25	0	1	0	1	0	0	1	1
26	–	–	–	–	–	–	–	–
27	–	–	–	–	–	–	–	–
28	–	–	–	–	–	–	–	–
29	–	–	–	–	–	–	–	–
30	–	–	–	–	–	–	–	–
31	–	–	–	–	–	–	–	–
32	0	1	0	1	0	0	1	1
33	0	1	0	1	0	0	1	1
34	0	1	0	1	0	1	0	0
35	0	1	0	1	0	1	0	0
36	0	1	0	1	0	1	0	0
37	0	1	0	1	0	1	0	1
38	0	1	0	1	0	1	0	1
39	0	1	0	1	0	1	0	1
40	0	1	0	1	0	1	1	0
41	0	1	0	1	0	1	1	0
42	–	–	–	–	–	–	–	–
43	–	–	–	–	–	–	–	–
44	–	–	–	–	–	–	–	–
45	–	–	–	–	–	–	–	–
46	–	–	–	–	–	–	–	–
47	–	–	–	–	–	–	–	–
48	0	1	0	1	0	1	1	0
49	0	1	0	1	0	1	1	1
50	0	1	0	1	0	1	1	1
51	0	1	0	1	0	1	1	1
52	0	1	0	1	1	0	0	0
53	0	1	0	1	1	0	0	0
54	0	1	0	1	1	0	0	0
55	0	1	0	1	1	0	0	1
56	–	–	–	–	–	–	–	–
57	–	–	–	–	–	–	–	–
58	–	–	–	–	–	–	–	–
59	–	–	–	–	–	–	–	–
60	–	–	–	–	–	–	–	–
61	–	–	–	–	–	–	–	–
62	–	–	–	–	–	–	–	–
63	–	–	–	–	–	–	–	–

The required divider range, 4800 to 5933, is obtained in the following manner: the MC12013 Dual Modulus Prescaler is connected in the divide by 10/11 mode; the modulus control counter uses two MC4016 stages with N_{mc} ranging from 00 to 99, establishing the two least significant digits of N_T. The remaining two digits of N_T are obtained from a three stage programmable counter generating N_{pc}. The least significant stage of the N_{pc} counter is fixed programmed to zero. The required programming for all remaining stages is derived from four channel selector BCD thumbwheel switches. The relationship between N_T and the counters is given by $N_T = MN_{pc} + N_{mc}$; for a typical channel, say 144.33 MHz, N_T = 4811 requires that M = 10, N_{pc} = 480, and N_{mc} = 11, or N_T = (10)(480) + 11 = 4811.

A general problem associated with synthesizer design arises from the fact that there is not always a one-to-one correspondence between the code provided by the channel selector switches and the code required for proper programming of the counters. For instance, in the example above where 144.33 MHz was selected, the channel selector switches are set to 44.33 while the required divider ratio is 4811. There are numerous solutions for a given translation requirement, however the method shown here using read only memories offers a straightforward design method. While field programmable read only memories (PROMs) are shown, they would normally be used only during development; suitable fixed ROMs are more economical in production quantities. The design procedure for the code conversion is illustrated in Figure 9. The required programming for the two most

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FIGURE 10 — N_{mc} PROM #1 PROGRAMMING

	SW #3	SW #4	SW #3 A5 A4	SW #4 A3 A2 A1 A0	PROM WORD	PROM OUTPUT M.S.B	PROM OUTPUT L.S.B.	N_{mc}
(144)	.00		0 0	0 0 0 0	0	0 0 0 0	0 0 0 0	00
	.03		0 0	0 0 1 1	3	0 0 0 0	0 0 0 1	01
	.06		0 0	0 1 1 0	6	0 0 0 0	0 0 1 0	02
	.09		0 0	1 0 0 1	9	0 0 0 0	0 0 1 1	03
	.12		0 0	0 0 1 0	18	0 0 0 0	0 1 0 0	04
	.15		0 0	0 1 0 1	21	0 0 0 0	0 1 0 1	05
	.18		0 0	1 0 0 0	24	0 0 0 0	0 1 1 0	06
	.21		0 0	0 0 0 1	33	0 0 0 0	0 1 1 1	07
	.24		0 0	0 1 0 0	36	0 0 0 0	1 0 0 0	08
	.27		0 0	0 1 1 1	39	0 0 0 0	1 0 0 1	09
	.30		0 0	1 0 0 0	48	0 0 0 1	0 0 0 0	10
	.33		0 0	1 0 1 1	51	0 0 0 1	0 0 0 1	11
	.36		0 0	0 1 1 0	54	0 0 0 1	0 0 1 0	12
	.39		0 0	1 0 0 1	57	0 0 0 1	0 0 1 1	13
	.42		0 1	0 0 1 0	2	0 0 0 1	0 1 0 0	14
	.45		0 1	0 0 0 1	5	0 0 0 1	0 1 0 1	15
	.48		0 1	0 0 0 0	8	0 0 0 1	0 1 1 0	16
	.51		0 1	0 0 0 1	17	0 0 0 1	0 1 1 1	17
	.54		0 1	0 1 0 0	20	0 0 0 1	1 0 0 0	18
	.57		0 1	0 1 1 1	23	0 0 0 1	1 0 0 1	19
	.60		0 1	1 0 0 0	32	0 0 1 0	0 0 0 0	20
	.63		0 1	0 0 1 1	35	0 0 1 0	0 0 0 1	21
	.66		0 1	0 1 1 0	38	0 0 1 0	0 0 1 0	22
	.69		0 1	1 0 0 1	41	0 0 1 0	0 0 1 1	23
	.72		0 1	1 0 1 0	49	0 0 1 0	0 1 0 0	24
	.75		0 1	1 1 0 1	53	0 0 1 0	0 1 0 1	25
	.78		0 1	1 1 1 0	56	0 0 1 0	0 1 1 0	26
	.81		1 0	0 0 0 1	1	0 0 1 0	0 1 1 1	27
	.84		1 0	0 1 0 0	4	0 0 1 0	1 0 0 0	28
	.87		1 0	0 1 1 1	7	0 0 1 0	1 0 0 1	29
	.90		1 0	0 0 0 0	16	0 0 1 1	0 0 0 0	30
	.93		1 0	0 0 1 1	19	0 0 1 1	0 0 0 1	31
	.96		1 0	0 1 1 0	22	0 0 1 1	0 0 1 0	32
(144)	.99		1 0	0 1 0 1	25	0 0 1 1	0 0 1 1	33

Use with frequency ranges:

144.00 – 144.99	162.00 – 162.99
147.00 – 147.99	165.00 – 165.99
150.00 – 150.99	168.00 – 168.99
153.00 – 153.99	171.00 – 171.99
156.00 – 156.99	174.00 – 174.99
159.00 – 159.99	177.00 – 177.99

WORD	BIT 7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0
1	0	0	1	0	0	1	1	1
2	0	0	0	1	0	1	0	0
3	0	0	0	0	0	0	0	1
4	0	0	1	0	1	0	0	0
5	0	0	0	1	0	1	0	1
6	0	0	0	0	0	0	1	0
7	0	0	1	0	1	0	0	1
8	0	0	0	1	0	1	1	0
9	0	0	0	0	0	0	1	1
10	–	–	–	–	–	–	–	–
11	–	–	–	–	–	–	–	–
12	–	–	–	–	–	–	–	–
13	–	–	–	–	–	–	–	–
14	–	–	–	–	–	–	–	–
15	–	–	–	–	–	–	–	–
16	0	0	1	1	0	0	0	0
17	0	0	0	1	0	1	1	1
18	0	0	0	0	0	1	0	0
19	0	0	1	1	0	0	0	1
20	0	0	0	1	1	0	0	0
21	0	0	0	0	0	1	0	1
22	0	0	1	1	0	0	1	0
23	0	0	0	1	1	0	0	1
24	0	0	0	0	0	1	1	0
25	0	0	1	1	0	0	1	1
26	–	–	–	–	–	–	–	–
27	–	–	–	–	–	–	–	–
28	–	–	–	–	–	–	–	–
29	–	–	–	–	–	–	–	–
30	–	–	–	–	–	–	–	–
31	–	–	–	–	–	–	–	–
32	0	0	1	0	0	0	0	0
33	0	0	0	0	0	1	1	1
34	–	–	–	–	–	–	–	–
35	0	0	1	0	0	0	0	1
36	0	0	0	0	1	0	0	0
37	–	–	–	–	–	–	–	–
38	0	0	1	0	0	0	1	0
39	0	0	0	0	1	0	0	1
40	–	–	–	–	–	–	–	–
41	0	0	1	0	0	0	1	1
42	–	–	–	–	–	–	–	–
43	–	–	–	–	–	–	–	–
44	–	–	–	–	–	–	–	–
45	–	–	–	–	–	–	–	–
46	–	–	–	–	–	–	–	–
47	–	–	–	–	–	–	–	–
48	0	0	0	1	0	0	0	0
49	0	0	1	0	0	1	0	0
50	–	–	–	–	–	–	–	–
51	0	0	0	1	0	0	0	1
52	–	–	–	–	–	–	–	–
53	0	0	1	0	0	1	0	1
54	0	0	0	1	0	0	1	0
55	–	–	–	–	–	–	–	–
56	0	0	1	0	0	1	1	0
57	0	0	0	1	0	0	1	1
58	–	–	–	–	–	–	–	–
59	–	–	–	–	–	–	–	–
60	–	–	–	–	–	–	–	–
61	–	–	–	–	–	–	–	–
62	–	–	–	–	–	–	–	–
63	–	–	–	–	–	–	–	–

significant digits of N_{pc} is shown versus the code provided by switches #1 and #2 of the channel selector. If the four outputs of switch #2 and the two least significant outputs of switch #1 are regarded as address bits A0 through A5 for a 64 x 8 TTL PROM, a memory location can be associated with each switch setting. The required N_{pc} programming for each switch setting is then set into the appropriate memory location by the user. In Figure 9, the required programming has been transferred into a truth table to be used while programming the PROM. A similar result for the N_{mc} programming is shown in Figure 10. Note that the PROM shown, N_{mc} PROM #1, selects only N_{mc} numbers 00 through 33. This means that the synthesizer as shown in Figure 8 selects only the adjacent channels in a one megahertz slice of the total band. The frequency ranges that can be selected using N_{mc} PROM #1 are summarized in Figure 10. For other ranges, N_{mc} PROM #1 must be replaced by one of two additional PROMs required for generating the remaining N_{mc} numbers. Appropriate truth tables along with the ranges they can be used with are shown in Figures 11 and 12.

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FIGURE 11 – N_{mc} PROM #2 TRUTH TABLE

WORD	BIT 7	6	5	4	3	2	1	0
0	0	1	1	0	0	0	0	0
1	0	1	0	0	0	1	1	1
2	0	0	1	1	0	1	0	0
3	0	1	1	0	0	0	0	1
4	0	1	0	0	1	0	0	0
5	0	0	1	1	0	1	0	1
6	0	1	1	0	0	0	1	0
7	0	1	0	0	1	0	0	1
8	0	0	1	1	0	1	1	0
9	0	1	1	0	0	0	1	1
10	–	–	–	–	–	–	–	–
11	–	–	–	–	–	–	–	–
12	–	–	–	–	–	–	–	–
13	–	–	–	–	–	–	–	–
14	–	–	–	–	–	–	–	–
15	–	–	–	–	–	–	–	–
16	0	1	0	1	0	0	0	0
17	0	0	1	1	0	1	1	1
18	0	1	1	0	0	1	0	0
19	0	1	0	1	0	0	0	1
20	0	0	1	1	1	0	0	0
21	0	1	1	0	0	1	0	1
22	0	1	0	1	0	0	1	0
23	0	0	1	1	1	0	0	1
24	0	1	1	0	0	1	1	0
25	0	1	0	1	0	0	1	1
26	–	–	–	–	–	–	–	–
27	–	–	–	–	–	–	–	–
28	–	–	–	–	–	–	–	–
29	–	–	–	–	–	–	–	–
30	–	–	–	–	–	–	–	–
31	–	–	–	–	–	–	–	–
32	0	1	0	0	0	0	0	0
33	–	–	–	–	–	–	–	–
34	0	1	0	1	0	1	0	0
35	0	1	0	0	0	0	0	1
36	–	–	–	–	–	–	–	–
37	0	1	0	1	0	1	0	1
38	0	1	0	0	0	0	1	0
39	–	–	–	–	–	–	–	–
40	0	1	0	1	0	1	1	0
41	0	1	0	0	0	0	1	1
42	–	–	–	–	–	–	–	–
43	–	–	–	–	–	–	–	–
44	–	–	–	–	–	–	–	–
45	–	–	–	–	–	–	–	–
46	–	–	–	–	–	–	–	–
47	–	–	–	–	–	–	–	–
48	–	–	–	–	–	–	–	–
49	0	1	0	1	0	1	1	1
50	0	1	0	0	0	1	0	0
51	–	–	–	–	–	–	–	–
52	0	1	0	1	1	0	0	0
53	0	1	0	0	0	1	0	1
54	–	–	–	–	–	–	–	–
55	0	1	0	1	1	0	0	1
56	0	1	0	0	0	1	1	0
57	–	–	–	–	–	–	–	–
58	–	–	–	–	–	–	–	–
59	–	–	–	–	–	–	–	–
60	–	–	–	–	–	–	–	–
61	–	–	–	–	–	–	–	–
62	–	–	–	–	–	–	–	–
63	–	–	–	–	–	–	–	–

Use with frequency ranges:

145.02 – 145.98
148.02 – 148.98
151.02 – 151.98
154.02 – 154.98
157.02 – 157.98
160.02 – 160.98
163.02 – 163.98
166.02 – 166.98
169.02 – 169.98
172.02 – 172.98
175.02 – 175.98

FIGURE 12 – N_{mc} PROM #3 TRUTH TABLE

WORD	BIT 7	6	5	4	3	2	1	0
0	1	0	0	0	0	0	0	0
1	0	1	1	0	0	1	1	1
2	1	0	0	1	0	1	0	0
3	1	0	0	0	0	0	0	1
4	0	1	1	0	1	0	0	0
5	1	0	0	1	0	1	0	1
6	1	0	0	0	0	0	1	0
7	0	1	1	0	1	0	0	1
8	1	0	0	1	0	1	1	0
9	1	0	0	0	0	0	1	1
10	–	–	–	–	–	–	–	–
11	–	–	–	–	–	–	–	–
12	–	–	–	–	–	–	–	–
13	–	–	–	–	–	–	–	–
14	–	–	–	–	–	–	–	–
15	–	–	–	–	–	–	–	–
16	0	1	1	1	0	0	0	0
17	1	0	0	1	0	1	1	1
18	1	0	0	0	0	1	0	0
19	0	1	1	1	0	0	0	1
20	1	0	0	1	1	0	0	0
21	1	0	0	0	0	1	0	1
22	0	1	1	1	0	0	1	0
23	1	0	0	1	1	0	0	1
24	1	0	0	0	0	1	1	0
25	0	1	1	1	0	0	1	1
26	–	–	–	–	–	–	–	–
27	–	–	–	–	–	–	–	–
28	–	–	–	–	–	–	–	–
29	–	–	–	–	–	–	–	–
30	–	–	–	–	–	–	–	–
31	–	–	–	–	–	–	–	–
32	–	–	–	–	–	–	–	–
33	1	0	0	0	0	1	1	1
34	0	1	1	1	0	1	0	0
35	–	–	–	–	–	–	–	–
36	–	–	–	–	–	–	–	–
37	0	1	1	1	0	1	0	1
38	1	0	0	0	1	0	0	0
39	1	0	0	0	1	0	0	1
40	0	1	1	1	0	1	1	0
41	–	–	–	–	–	–	–	–
42	–	–	–	–	–	–	–	–
43	–	–	–	–	–	–	–	–
44	–	–	–	–	–	–	–	–
45	–	–	–	–	–	–	–	–
46	–	–	–	–	–	–	–	–
47	–	–	–	–	–	–	–	–
48	1	0	0	1	0	0	0	0
49	0	1	1	1	0	1	1	1
50	–	–	–	–	–	–	–	–
51	1	0	0	1	0	0	0	1
52	0	1	1	1	1	0	0	0
53	–	–	–	–	–	–	–	–
54	1	0	0	1	0	0	1	0
55	0	1	1	1	1	0	0	1
56	–	–	–	–	–	–	–	–
57	1	0	0	0	0	0	1	1
58	–	–	–	–	–	–	–	–
59	–	–	–	–	–	–	–	–
60	–	–	–	–	–	–	–	–
61	–	–	–	–	–	–	–	–
62	–	–	–	–	–	–	–	–
63	–	–	–	–	–	–	–	–

Use with frequency ranges:

146.01 – 146.97
149.01 – 149.97
152.01 – 152.97
155.01 – 155.97
158.01 – 158.97
161.01 – 161.97
164.01 – 164.97
167.01 – 167.97
170.01 – 170.97
173.01 – 173.97
176.01 – 176.97